LISTING OF CLAIMS:

The following listing of claims replaces all previous versions and listings of claims in the present application.

Please cancel claims 1-7.

1.-7. (Canceled)

8. (New) A vertical MOS device having a trench gate structure, the semiconductor device comprising:

a semiconductor body having a trench, the trench having an inlet, a sidewall and a bottom;

a gate insulation film disposed to cover the sidewall and the bottom of the trench, the gate insulation film comprising a laminate structure of a first silicon oxide film, silicon nitride film and a second silicon oxide film successively laminated in this order from a trench side; and

a gate electrode of a polycrystalline silicon which is doped with boron, the gate electrode filling the trench with the gate insulation film interposed, wherein:

the semiconductor body has a first region of a first conductivity type, a second region of a second conductivity type, and a third region of the first conductivity type vertically aligned along the trench, and thereby a vertical MOS structure is formed by the gate electrode in the trench, the gate insulation film on the sidewall of the trench, and the first through third region;

the laminate structure of the gate insulation film is disposed to cover at least the second region in the trench;

the silicon nitride film in the laminate structure has a film thickness and film quality sufficient for suppressing boron from passing through the silicon nitride film; and

the first silicon oxide film at the trench side in the laminate structure has a film thickness that is greater than a film thickness of the second silicon oxide film at the gate electrode side.

9. (New) The vertical MOS device according to claim 8, wherein the first conductivity type is P-type, the second conductivity type is N-type, and the vertical MOS structure is a P channel type MOSFET.

10. (New) The vertical MOS device according to claim 8, wherein the silicon nitride film in the laminate structure has a film thickness of 10-30 nm.

11. (New) The vertical MOS device according to claim 8, wherein the first silicon oxide film in the laminate structure has a film thickness of approximately 100 nm.

12. (New) The vertical MOS device according to claim 8, wherein the film thickness of the first silicon oxide film in the laminate structure is controlled to satisfy a withstand voltage required for the laminate structure per se.

13. (New) The vertical MOS device according to claim 8, wherein the silicon nitride film is a deposited film.

14. (New) The vertical MOS device according to claim 8, wherein the laminate structure of the gate insulation film is locally located on the sidewall of the trench, and the gate insulation film comprises a first thick silicon oxide film disposed on the bottom of the trench, the first thick silicon oxide film having a film thickness greater than a film thickness of the laminate structure and covering a corner of the bottom of the trench.

15. (New) The vertical MOS device according to claim 8, wherein the laminate structure of the gate insulation film is locally located on the sidewall of the trench, and the gate insulation film comprises a second thick silicon oxide film disposed on the inlet of the trench, the second thick silicon oxide film having a film thickness greater than a film thickness of the laminate structure and covering an inlet corner of the trench.

16. (New) The vertical MOS device according to claim 14, wherein the laminate structure of the gate insulation film is locally located on the sidewall of the trench, and on the inlet of the trench is disposed a second thick silicon oxide film as the gate insulation film, the second thick silicon oxide film having a film thickness greater than the film thickness of the laminate structure and covering an inlet corner of the trench.

17. (New) A vertical MOS device having a trench gate structure, the semiconductor device comprising:

a semiconductor body having a trench, the trench having an inlet, a sidewall and a bottom;

a gate insulation film disposed to cover the sidewall and the bottom of the trench, the gate insulation film comprising a laminate structure of a first silicon oxide film, silicon nitride film of 10-30 nm in thickness and a second silicon oxide film successively laminated in this order from a trench side; and

a gate electrode of a polycrystalline silicon which is doped with boron, the gate electrode filling the trench with the gate insulation film interposed, wherein:

the semiconductor body has a first region of a first conductivity type, a second region of a second conductivity type, and a third region of the first conductivity type vertically aligned along the trench, thereby forming a vertical MOS structure by the gate electrode in the trench, the gate insulation film on the sidewall of the trench, and the first through third region;

the laminate structure of the gate insulation film is disposed to locally cover the sidewall of the trench;

the first silicon oxide film at the trench side in the laminate structure has a film thickness that is greater than a film thickness of the second silicon oxide film at the gate electrode side; and

the gate insulation film on the bottom of the trench is a first thick silicon oxide film which has a film thickness greater than a film thickness of the laminate structure, the first thick silicon oxide film covering a corner of the bottom of the trench.

18. (New) The vertical MOS device according to claim 17, wherein the first silicon oxide film in the laminate structure has a film thickness of approximately 100 nm.

19. (New) The vertical MOS device according to claim 17, wherein the inlet of the trench is covered with a second thick silicon oxide film which has a film thickness greater than the film thickness of the laminate structure and covers an inlet corner of the trench.